Imsys thesis proposals

Imsys AB
Johanneslundsvägen 3
Upplands Väsby
SE-194 61 Sweden
Phone:
+46 8 594 110 70
Mail: info@imsystech.com
Web: imsystech.com

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1. About Imsys, processors and accelerators

Imsys is a Swedish-based designer, developer, and supplier of networked control solutions for embedded systems, telematics, automation as well as in the Internet of Things (IoT). Our products range from processor components, computer-on-modules (COMs), and multipurpose modules to development kits and IP cores.

In the last 40 years of microprocessor development, much has changed, but the focus has always remained the same: creating smaller devices with increased speed, memory, and power. 16-bit became 32-bit, which gave way to today's 64-bit multi-core processors. The dominant paradigm has always been that more is more.

Imsys supplies MCUs, microcontroller units, and modules to original equipment and design manufacturers as well as application developers. Our customers represent a wide array of different industries and areas of technology, and today Imsys technology can be found in all types of devices in every corner of the globe.

Founded in 1981, Imsys has long pioneered unique and efficient new uses for microprocessor technology in the market. The earliest versions of our processors were used in data terminal systems as well as office computers, before being adapted for use with scanner controllers and document image processing systems. In the 1990s, Imsys played a role in developing new technology to greatly reduce the cost and increase the functionality of laser printer controllers.

Imsys is powering the increased demand for processing at the network edge and in smart sensors. Efficient AI processing and in particular inference using neural networks, is supported with a many core accelerator based on the proven and flexible Imsys core.

2. Master thesis proposals

Power efficient near memory computing for NN inference

Near processing memory and low power scheduling strategies.

Tensor organization for distributed memories with their associated processing element

Data distribution. Data (re)organization. Sequencing to match memory sizes. Feature map depth splitting.

Strategies for processing fully connected neural network layers in a fully distributed architecture

Data exchange schemes. Duplication for speed. 5 tier memory hierarchy strategies.

Weight compression technologies in an accelerator array.

Quantization, pruning, data representation, weight sharing & post multiplication, bit-plane compression.

Acceleration of Java based image processing library.

Advanced preprocessing of data before NN analysis. Challenge algorithm distribution on manycore. Systemize selected algorithms.

3. Bachelor thesis proposals (team effort)

Radar demonstrator on Imsys FPGA based neural network accelerator emulator.

Classify and track objects. Sensor fusion. Vertically optimized code down to micro code.

Real time 2D FFT demonstrator on Imsys accelerator

Camera on host computer. Present FFT picture on monitor in real time.

Intelligent door opener.

Identify pedestrians from image sensor, track them, infer intention, identify individuals, door acts on intention and identity.

Implementation of TI MSP430 in microcode.

Demonstrate efficiency and flexibility of parallel micro coding with reference from embench.org

Efficient abstract CISC ISA for neural network acceleration.

Implementation in parallel and flexible microcode with a reference from ONNX interchange format.